CLAIMS

What is claimed is:

1. An ATM-Ethernet network system, comprising:

an ATM processor;

an Ethernet network processor; and

an ATM-Ethernet processor interfacing between the ATM processor and the Ethernet network processor, the ATM-Ethernet processor including:

a packet buffer pointer ring for managing traffic from the Ethernet network processor to the ATM processor, the packet buffer pointer ring to contain a plurality of ATM processor packet buffer pointers,

a packet descriptor ring and a data buffer for managing traffic from the ATM processor to the Ethernet network processor, the packet descriptor ring being configured to contain a plurality of packet descriptors each including an ATM-Ethernet packet buffer memory address in the data buffer.

2. The system of claim 1, further comprising SONET framer, wherein the ATM processor is an ATM L2 processor in communication with the SONET framer.

3. The system of claim 1, further comprising an Ethernet MAC in communication with the Ethernet network processor.

4. The system of claim 1, wherein the packet buffer pointer ring is hardware scalable in size.

5. The system of claim 4, wherein the packet buffer pointer ring is a hardware FIFO to contain packet buffer pointers that point to packet buffer memory locations in the memory of the ATM processor.

6. The system of claim 1, wherein each packet buffer pointer contains a flag to signal to the ATM-Ethernet processor hardware whether the packet buffer pointer is being used.

7. The system of claim 1, wherein each packet buffer pointer points to a packet buffer memory location in a memory of the ATM processor.

8. The system of claim 1, wherein each packet buffer pointer contains 16 bits, 15 of which being for a pointer to point to a packet buffer memory location in a memory of the ATM processor.

9. The system of claim 1, wherein the packet buffer pointer ring and the packet descriptor ring are implemented as circular FIFOs.

10. A method for data communication, comprising:

receiving a packet from a network processor by an ATM-Ethernet processor for transmission to an ATM processor;

fetching a packet buffer pointer from a packet buffer pointer ring of the ATM-Ethernet processor, the packet buffer pointer including a memory address pointing to a packet buffer memory location in a data buffer memory of the ATM processor; and

transmitting the fetched packet buffer pointer and the received packet to the ATM processor.

11. The method of claim 10, further comprising:

identifying the memory in the ATM processor to which the memory address in the fetched packet buffer pointer points by the ATM processor;

storing the packet to the memory identified in the ATM processor; and

returning the packet buffer pointer to the ATM-Ethernet processor for reuse.

12. The method of claim 11, wherein said returning is performed after transmitting the data in the packet from the ATM processor to a SONET framer.

13. The method of claim 10, wherein the packet buffer pointer ring of the ATM-Ethernet processor is hardware scalable in size.

14. The method of claim 10, wherein the packet buffer pointer contains a flag to signal to the ATM-Ethernet processor hardware whether the packet buffer pointer is being used.

15. The method of claim 10, wherein the packet buffer pointer ring is implemented in the ATM-Ethernet processor as a circular FIFO.

16. A method for data communication, comprising:

receiving a packet from an ATM processor by an ATM-Ethernet processor for transmission to a network processor;

storing the packet in a data buffer of the ATM-Ethernet processor;

storing a packet descriptor for the packet in a packet descriptor ring of the ATM-Ethernet processor, the packet descriptor including a pointer to a memory location in the data buffer to which the packet is stored;

analyzing the packet descriptor for error; and

if error is detected:

dropping the packet descriptor;

reporting error to the ATM processor;

if no error is detected:

fetching the packet from the data buffer of the ATM-Ethernet processor; and

transmitting the packet to the network processor.

17. The method of claim 16, further comprising returning the packet descriptor to the packet descriptor ring for reuse.

18. The method of claim 16, wherein the packet descriptor ring of the ATM-Ethernet processor is hardware scalable in size.

19. The method of claim 16, wherein the packet descriptor ring is implemented in the ATM-Ethernet processor as a circular FIFO.

20. The method of claim 16, wherein the packet descriptor contains 8 bytes.